

# **SOI Materials for Silicon IC Technology**

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# Outline

- **Why SOI?**
- **SOI Materials & Processes**
  - SIMOX and Bonded
- **Characterization of SOI Materials**
  - Physical & Electrical
- **CMOS Technology on SOI**
  - $0.22 \rightarrow 0.18 \rightarrow 0.13 \mu\text{m} \rightarrow 0.1 \mu\text{m}$
- **Advanced SOI Materials**
  - Strained-Si on SOI
  - Patterned SOI
- **Future Directions**
  - 300 mm Development
  - Thickness and Thickness Uniformity Requirements for 0.13 um & Beyond CMOS Technologies

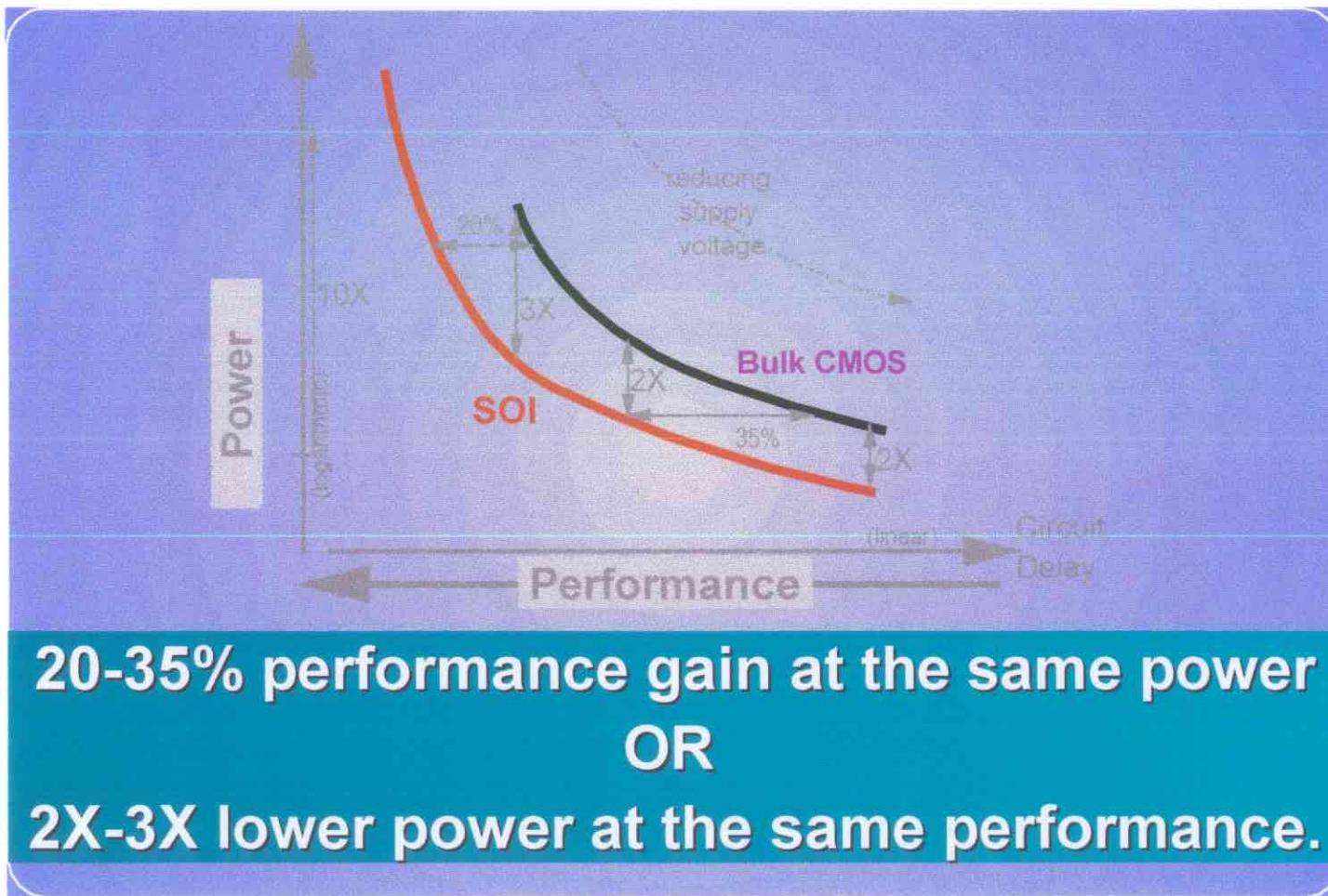
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# Why SOI?

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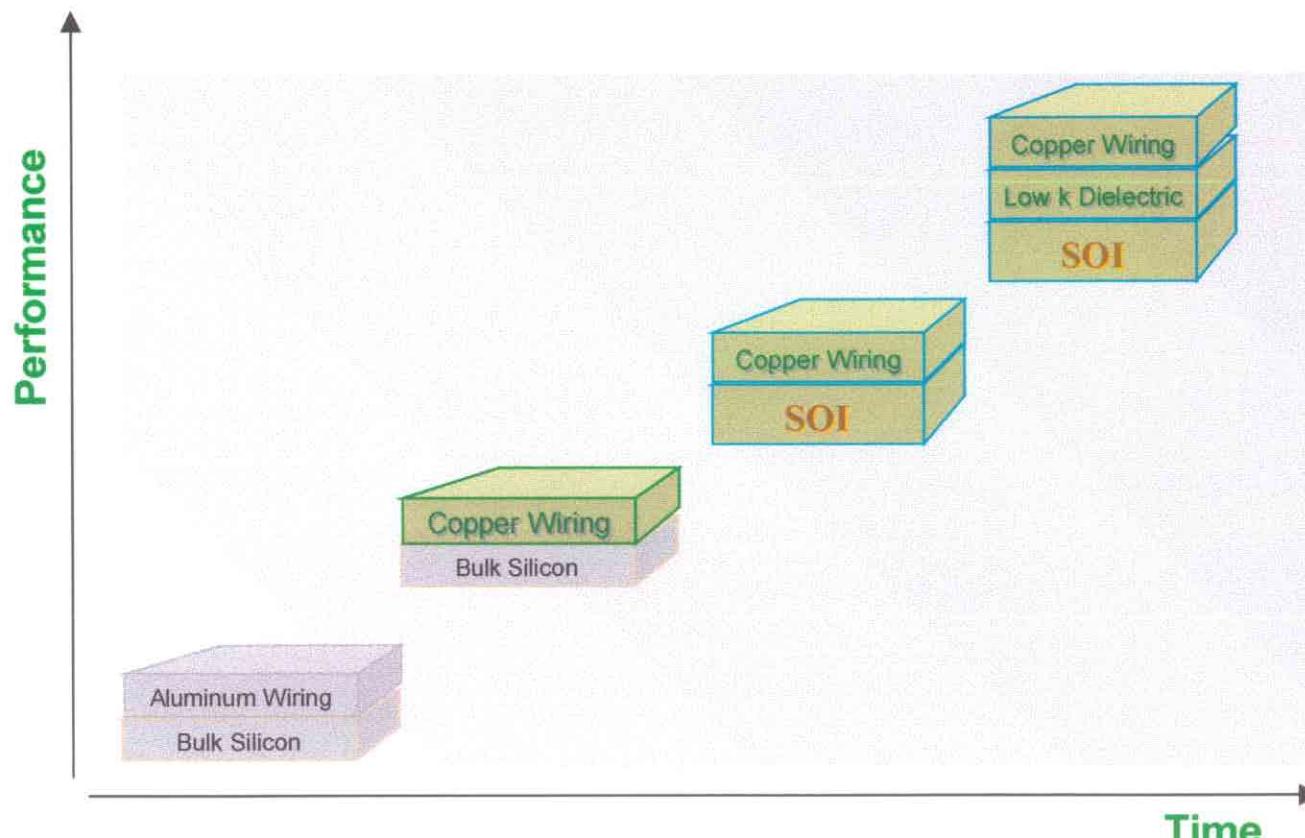
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# The Performance vs. Power Tradeoff



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# Technology Migration Roadmap

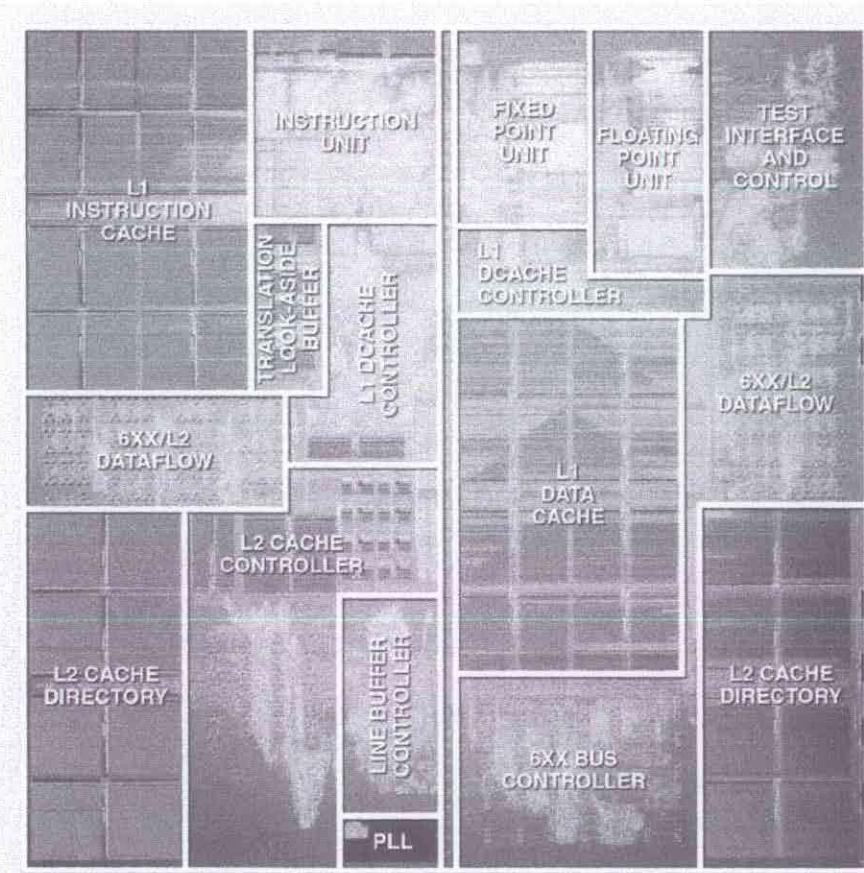


**SOI, Copper and low-k dielectrics are complimentary technologies.**

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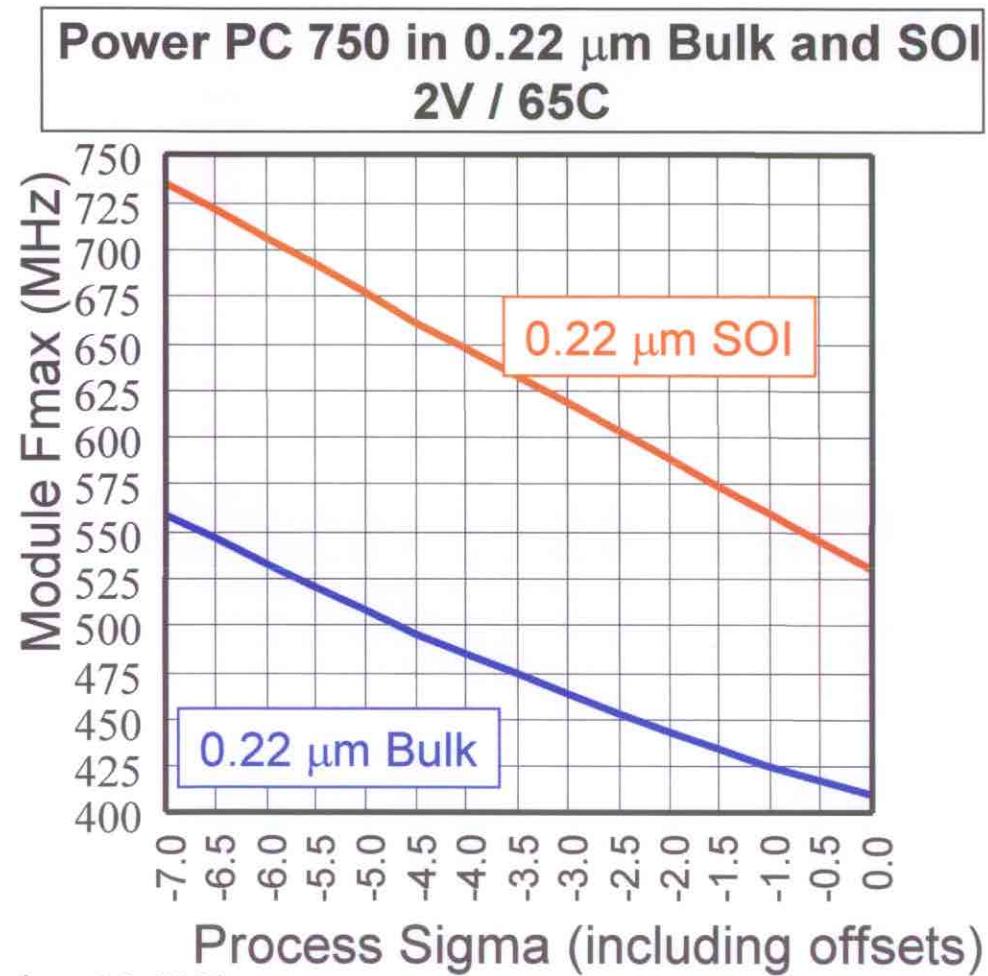
# 64-bit PowerPC on SOI



Nearly 30 million transistors  
7S (0.22 um ) Technology

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# Hardware Result



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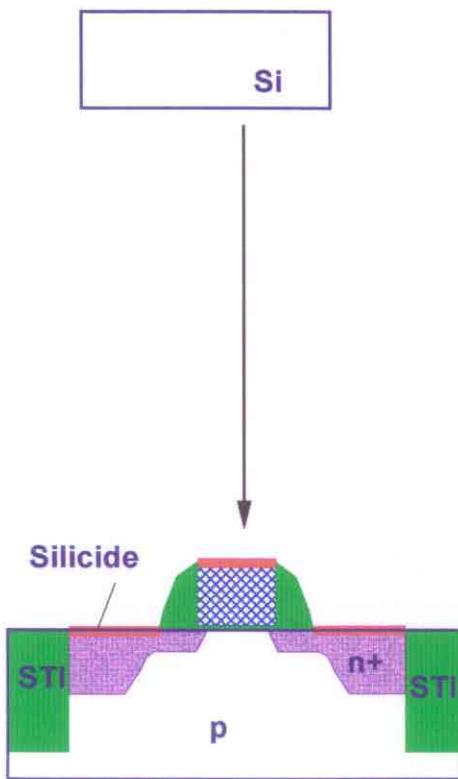
# **SOI Materials & Processes**

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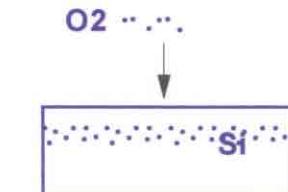
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# SOI Process

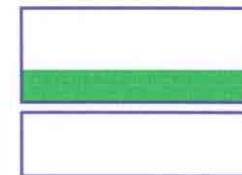
- In Bulk CMOS:



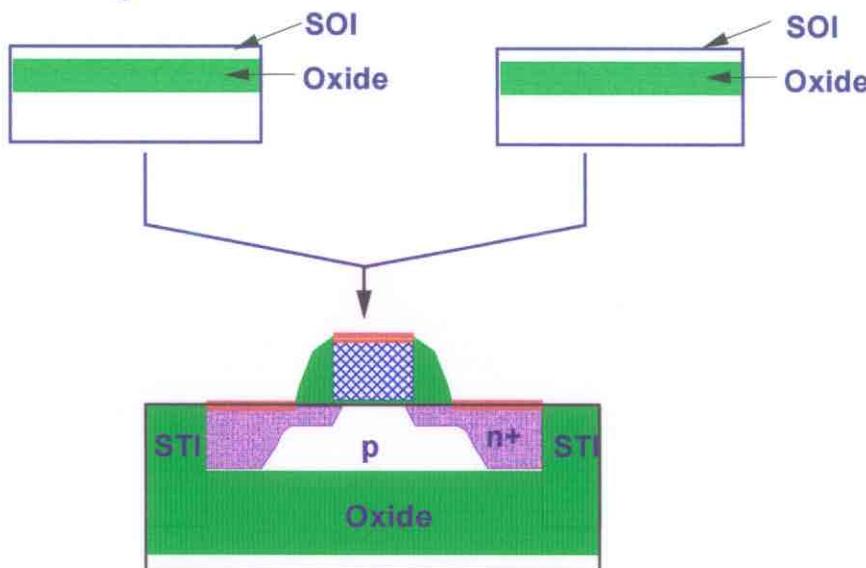
- Implant Si with Oxygen:



- SOI through bonding



- Anneal damage:



- Same lithography and tool set as existing bulk technologies
- Same metallization

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# Commercial SOI Material Choices

- **Bonded SOI**
  - H+ Induced Cleave
  - Porous Si Induced Cleave
  - Nano Cleave
  - Mechanical Thinning
  - Bond & Etchback
- **SIMOX**
  - Low Dose
  - Medium Dose
  - Standard Dose
  - MLD (Modified Low Dose)

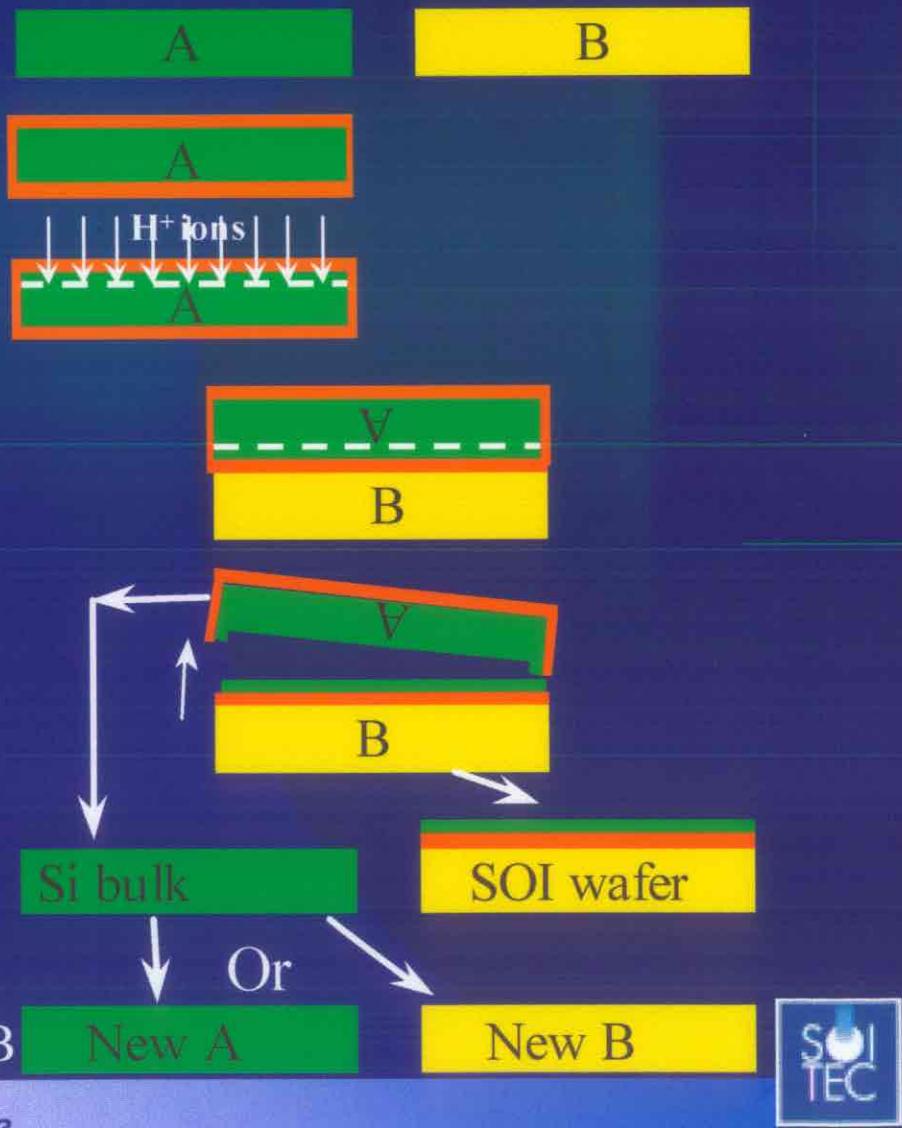
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# Bonded SOI Variables

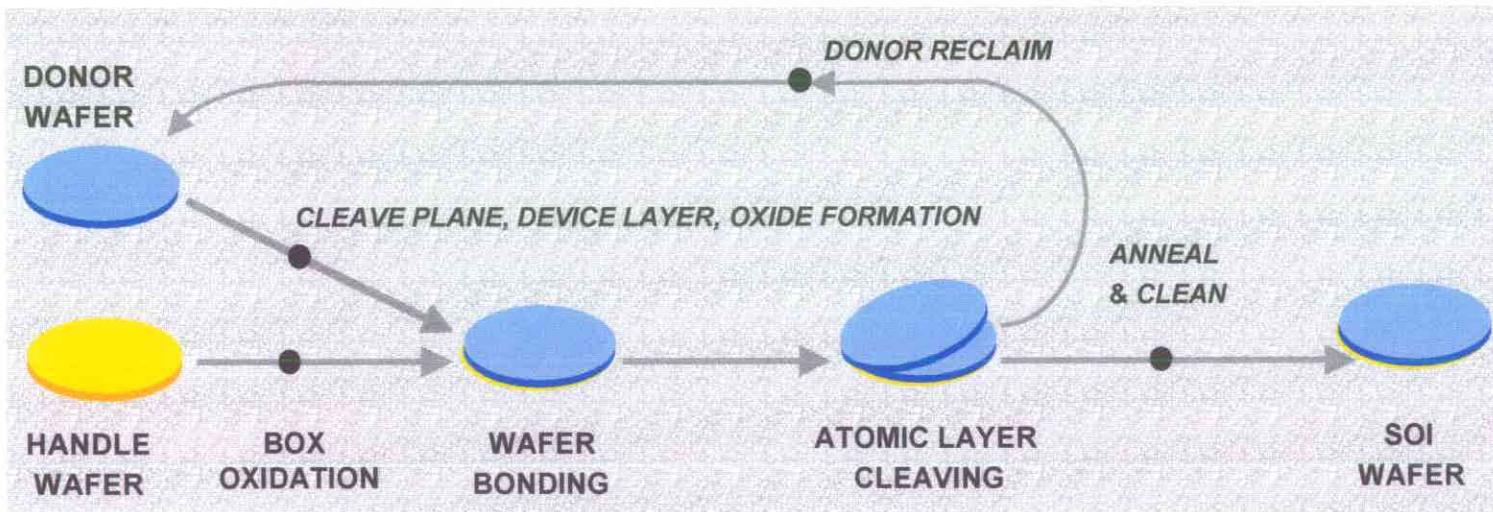
- Bonding Interface
  - $\text{SiO}_2 \rightarrow \text{Si}$
  - $\text{SiO}_2 \rightarrow \text{SiO}_2$
  - $\text{Si} \rightarrow \text{SiO}_2$
- Bonding Temperature
  - RT to 1200C
- Superficial Si Preparation
  - Layer Transfer + CMP or H<sub>2</sub> anneal
    - H+ implant induced
    - Porous-Si induced
    - H+/Si-Ge induced
  - Etch stop + grinding + CMP+ touch polish
  - Grinding + CMP+ touch polish

# UNIBOND™ Process Flow

- ① Initial Silicon
- ② Oxidation
- ③ Smart Cut® implantation
- ④ Cleaning & Bonding
- ⑤ Smart Cut® splitting
- ⑥ Annealing 1100°C & CMP Touch polish
- ⑧ Wafer A becomes new A or B



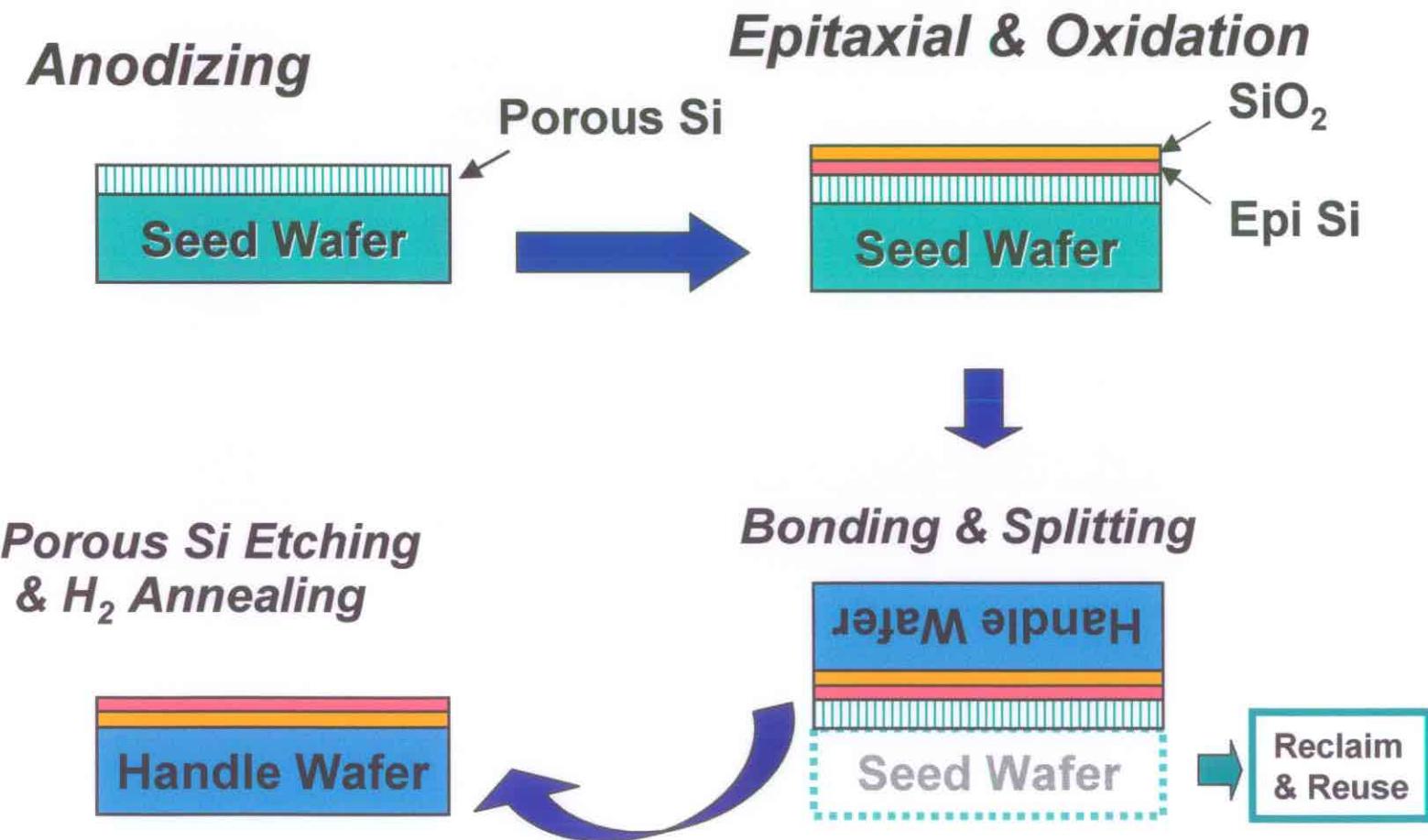
# SiGen NanoCleave™ SOI Wafer Process



- Sub-Nanometer as-cleaved roughness (1-3 Å RMS)
  - As-cleaved, usable product: RMS~1 Å
  - **NO CMP steps, NO edge polish**
- Extensions to Ge-rich layers with modest process change

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# ELTRAN® SOI-Epi Wafer™ fabrication process

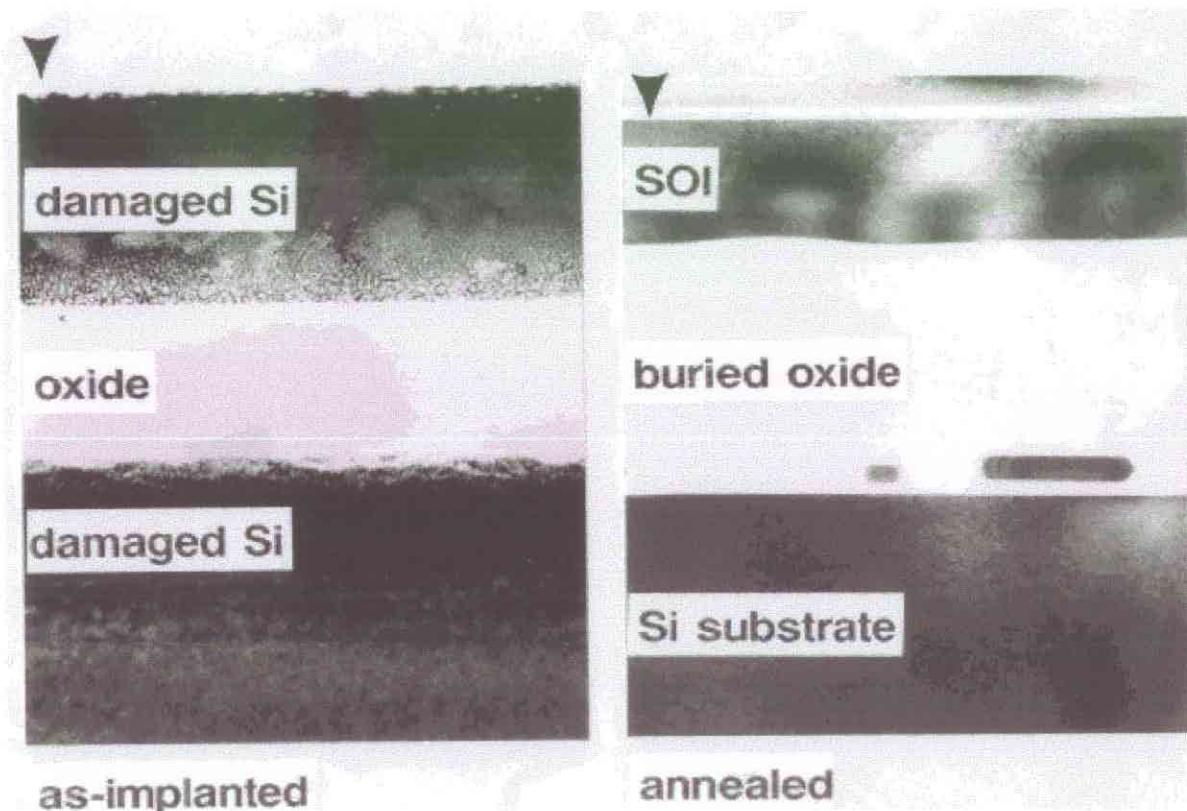


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# **SIMOX Material Variables**

- **Energy: 60-200 keV**
- **Dose**
  - Low:  $2\text{E}17\text{-}7\text{E}17 \text{ cm}^{-2}$
  - Medium:  $8\text{E}17\text{-}1.2\text{E}18 \text{ cm}^{-2}$
  - High (Std):  $1.8\text{-}2.2\text{E}18 \text{ cm}^{-2}$
- **Imp Temp: 450-620C**
- **Anneal Temp: 1300-1375**
- **Anneal Time: 4-24 hrs**
- **ITOX vs no ITOX**
- **Anneal Type: capped or uncapped**

## XTEM of Standard Dose SIMOX

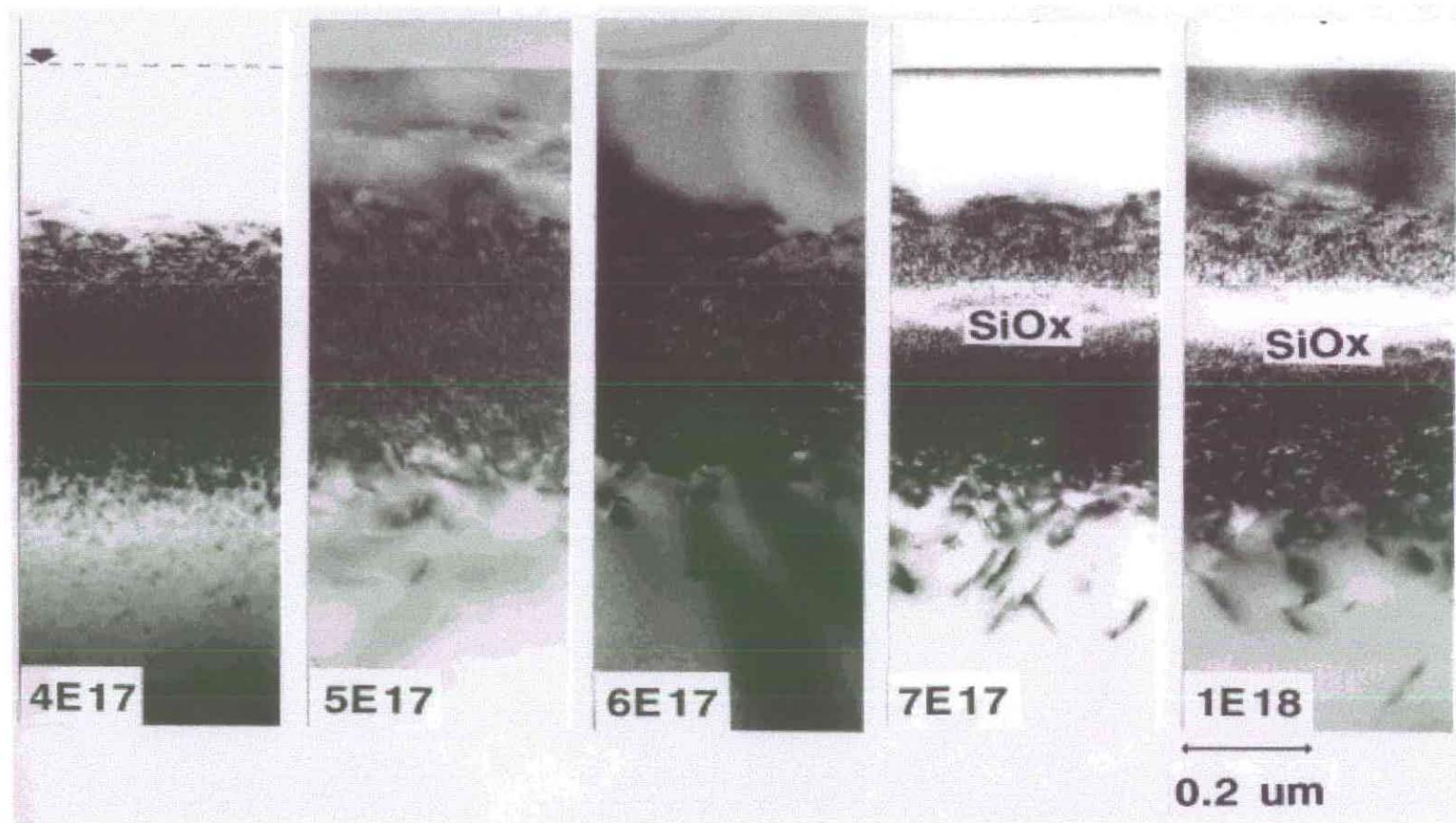


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## XTEM of As-Implanted SIMOX as a Function of O<sup>+</sup> Dose

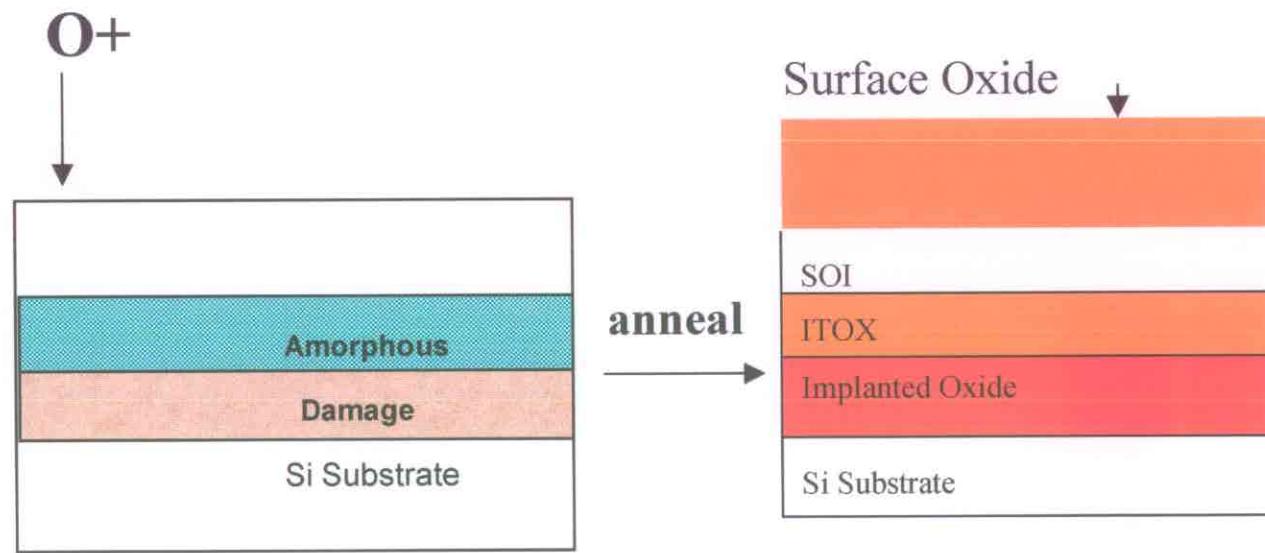


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## MLD SIMOX Process



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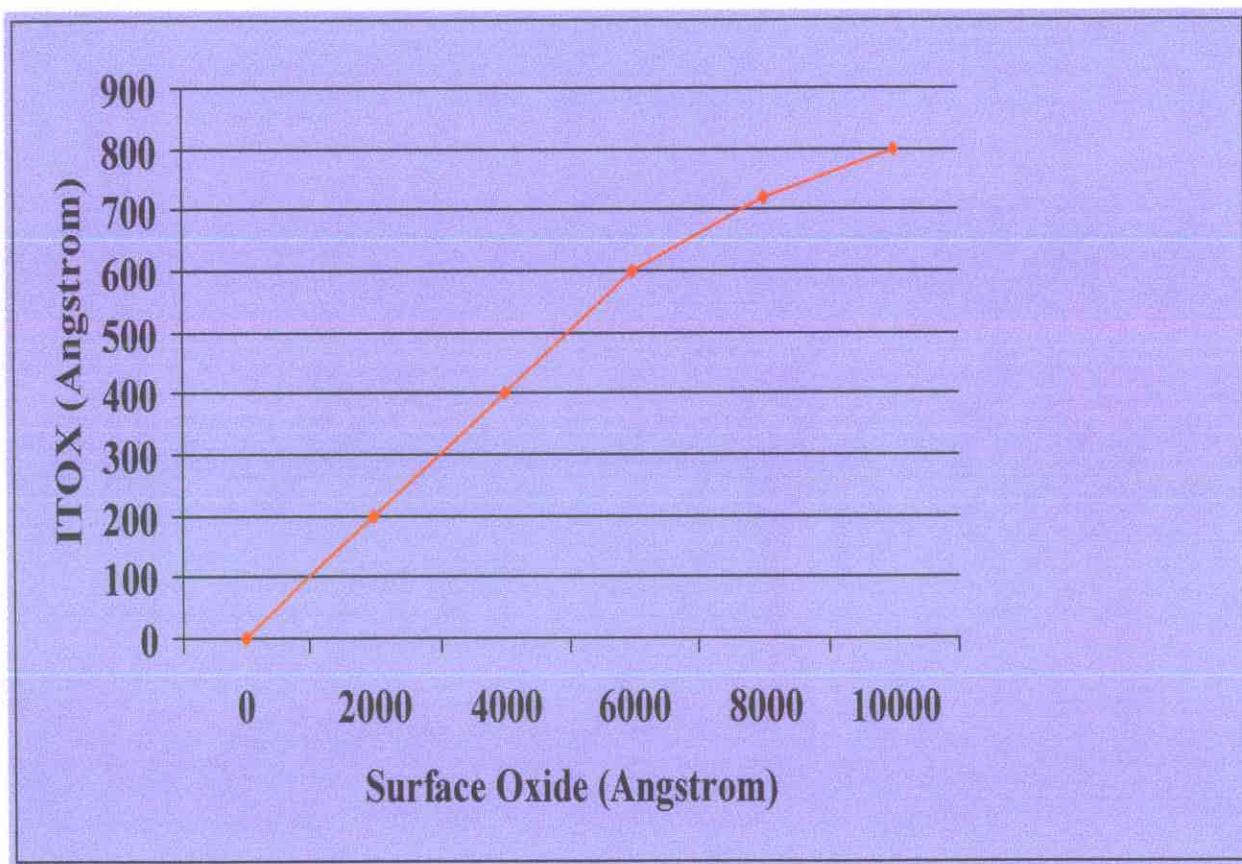
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## What is ITOX?

- ITOX is Internal Thermal OXidation in Silicon
- When Si is oxidized it forms an oxide layer at the surface. Simultaneously, however, a small fraction of oxygen (8-10%) diffuses into the Si
- This phenomenon is more evident in SOI wafers especially those oxidized at very high temperatures (> 1300C)
- The diffused oxygen grows an additional oxide layer on top of the existing BOX which is measurable by standard characterization techniques (SE, XTEM, XSEM etc)

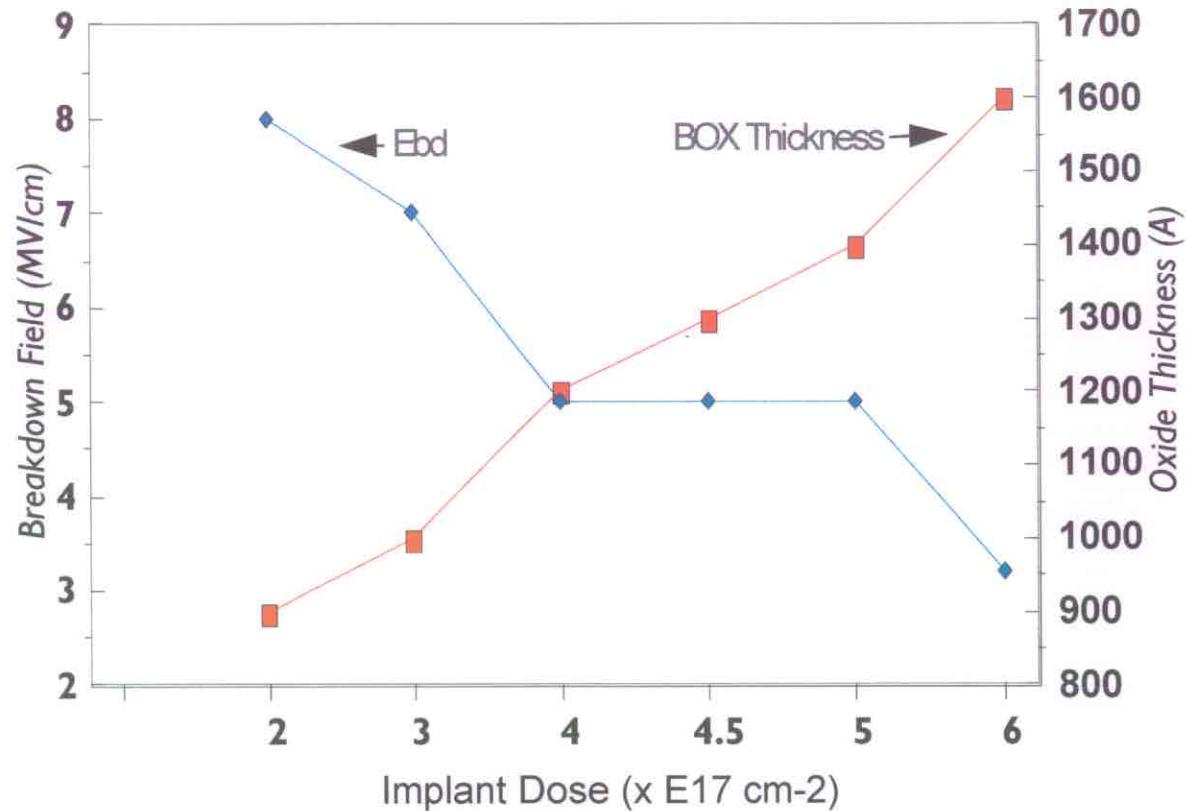
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## Surface Oxide vs ITOX Growth in SIMOX (~1350C)



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## BOX Quality Improves as O<sup>+</sup> Dose Decreases in MLD SIMOX

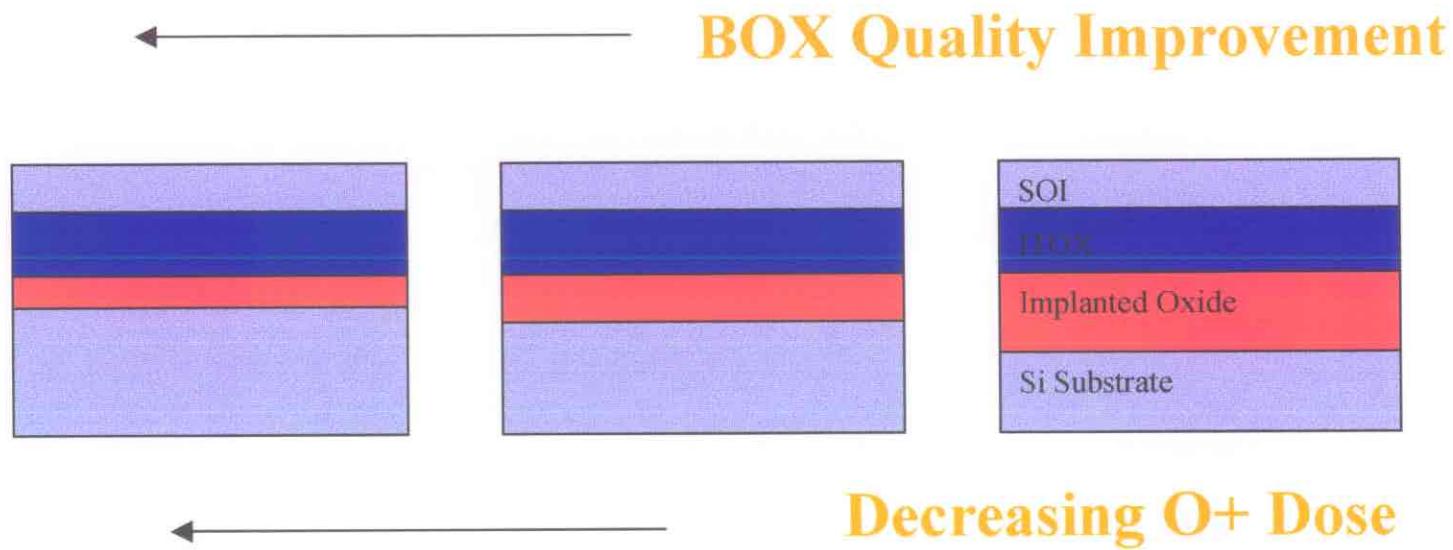


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# Schematics of Implanted and ITOX Induced Oxides with Increasing Oxygen Dose



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# SOI Material Characterization

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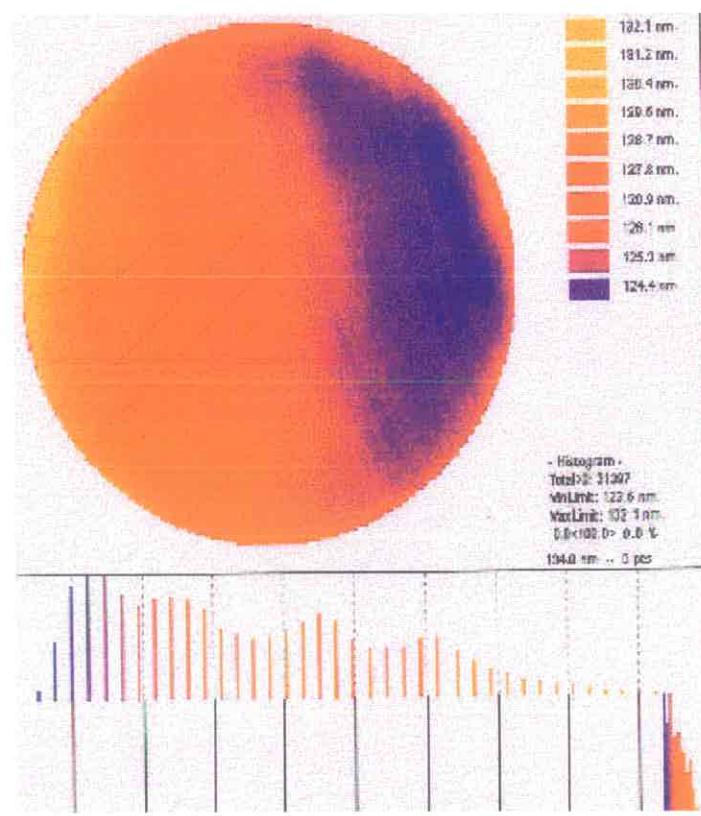
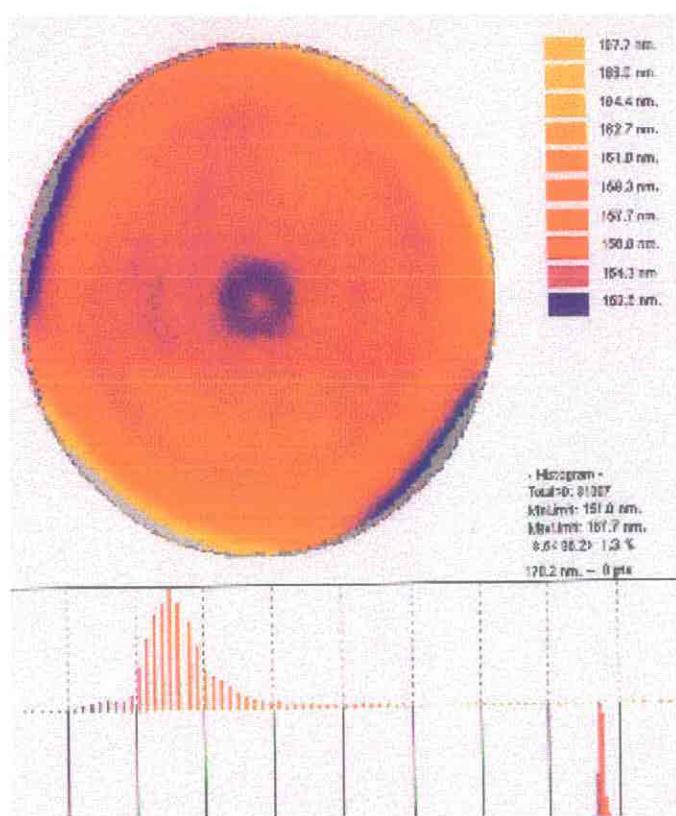
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# SOI Wafers : Physical Analysis

## ■ Screening Parameters

- HF-Defects (*49% HF dip, >/= 30 min*)
- Dislocations (*secco etch/optical microscopy, TEM*)
- Surface Roughness (*AFM*)
- Surface Pits (*AFM*)
- Slip (*Magic Mirror, Hologenix*)
- Metal levels (*TXRF, SIMS, AAAS, ICPMS*)
- Particles (*>/= 0.16 um, commercial particle mappers*)
- Thickness and thickness uniformity (*ellipsometry, optical reflection based mapping*)
- BOX thickness and thickness uniformity (*ellipsometry, optical reflection based mapping*)

## Typical Thickness Uniformity in Bonded SOI and MLD SIMOX

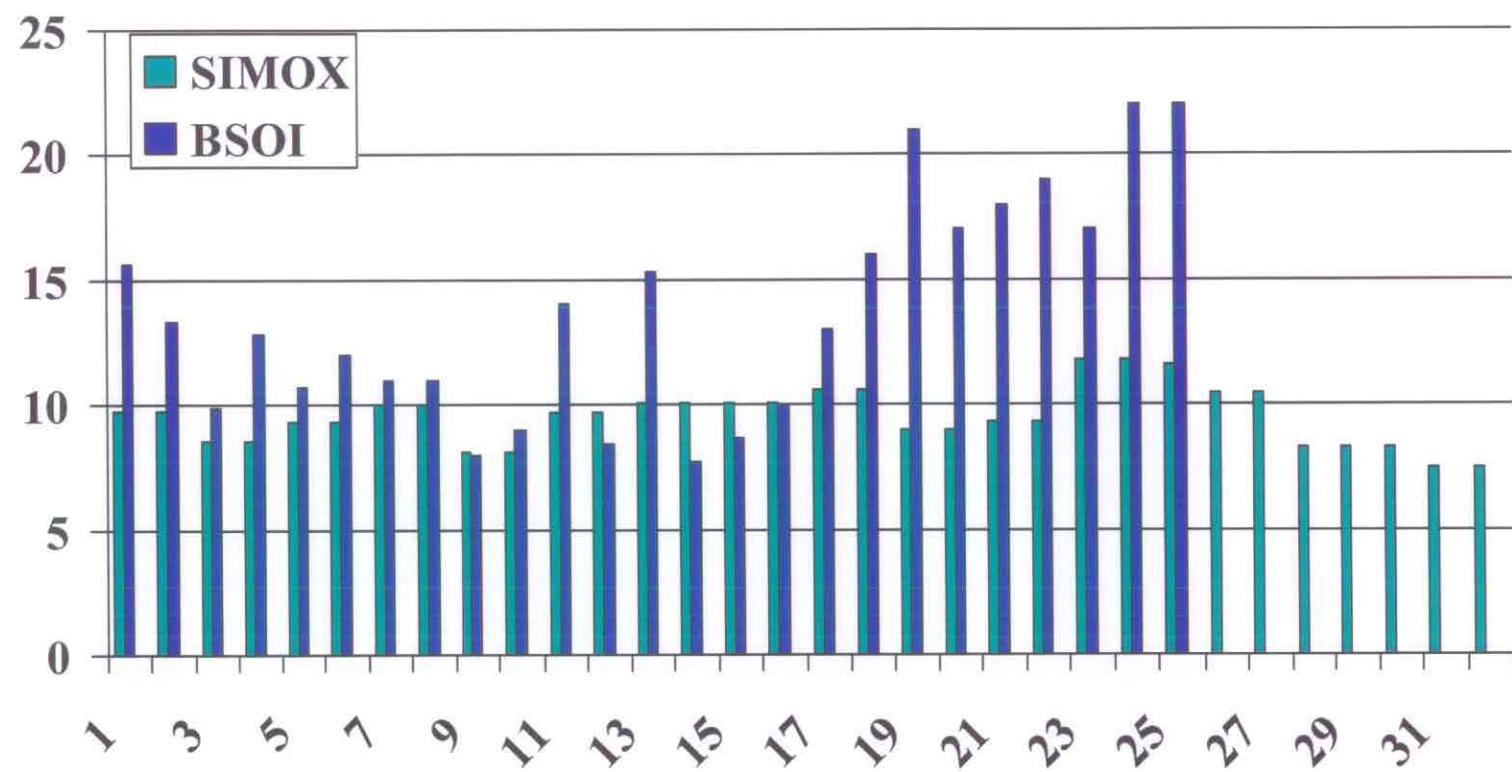


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## Comparison of Standard Deviations in SIMOX and Bonded SOI



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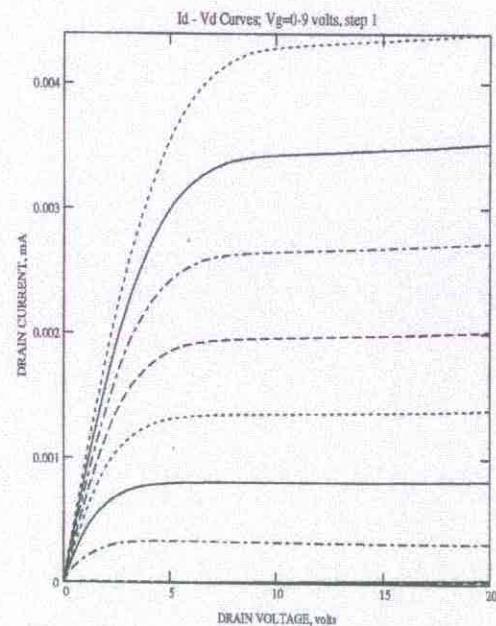
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# SOI Wafers : Electrical Analysis

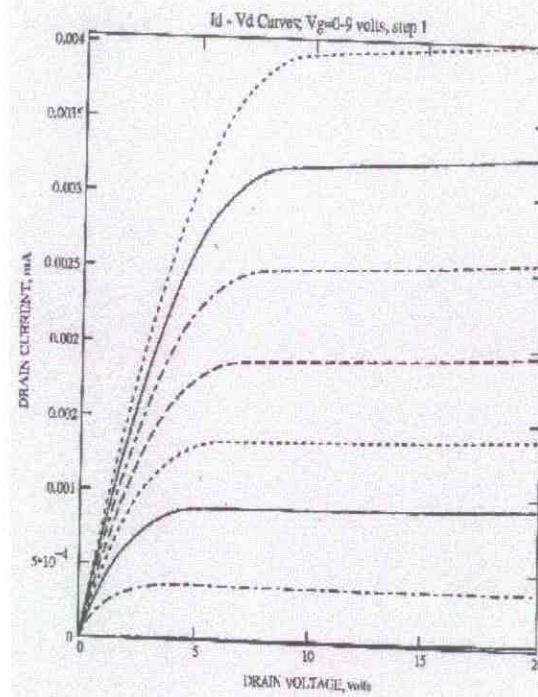
## ■ Screening Parameters (Electrical)

- MOS characteristics
  - ▶ *Threshold voltage*
  - ▶ *electron/hole mobilities*
  - ▶ *Transconductance*
  - ▶ *Output conductance*
  - ▶ *BOX charge*
  - ▶ *Floating body effects*
- BOX Integrity (*Vbd, Qbd, short density, leakage*)
- Gate Oxide Integrity (*Vbd, Qbd..*)
- Minority carrier lifetime (*microwave reflection based*)

# Id-Vd Plots of MLD SIMOX and Bonded SOI by HgFET



HgFET Id-Vd Curves; UniBond; Si = 1149Å, BOX = 1434Å.



HgFET Id-Vd Curves; SIMOX; Si = 1485Å, BOX = 1473Å.

# **CMOS Technology on SOI**

## **0.22→0.10 um**

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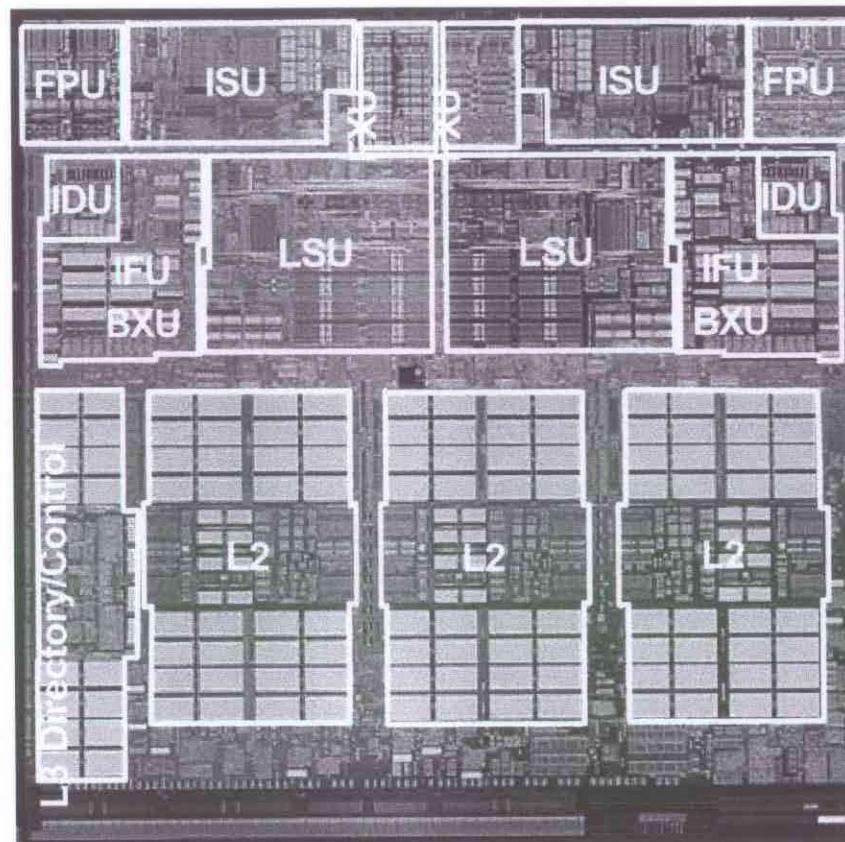
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## IBM CMOS Technology Evolution

	5X	6X	7S	7S-SOI	8S	8S2	8SF	9S	9S2
Production	94	97	98	98	99	00	01	01	02
Generation	0.35	0.25	0.22	0.22	0.18	0.18	0.13	0.13	0.13
Gate Length	0.35	0.18	0.15	0.14	0.1	0.09	0.07		
SRAM Cell	33	15	6.8	6.8	4.2	4.2	2.48	2.16	1.8
Device	Bulk	Bulk	Bulk	SOI	Bulk	SOI	Bulk	SOI	SOI
Metal	5 / Al	6 / Al	6 / Cu	6 / Cu	7 / Cu	7 / Cu	8 / Cu	9 / Cu	9 / Cu
Metal Dielectric Improvement	1	1	1	1	1	1.1	1.3	1.3	1.4

# Power 4 Microprocessor



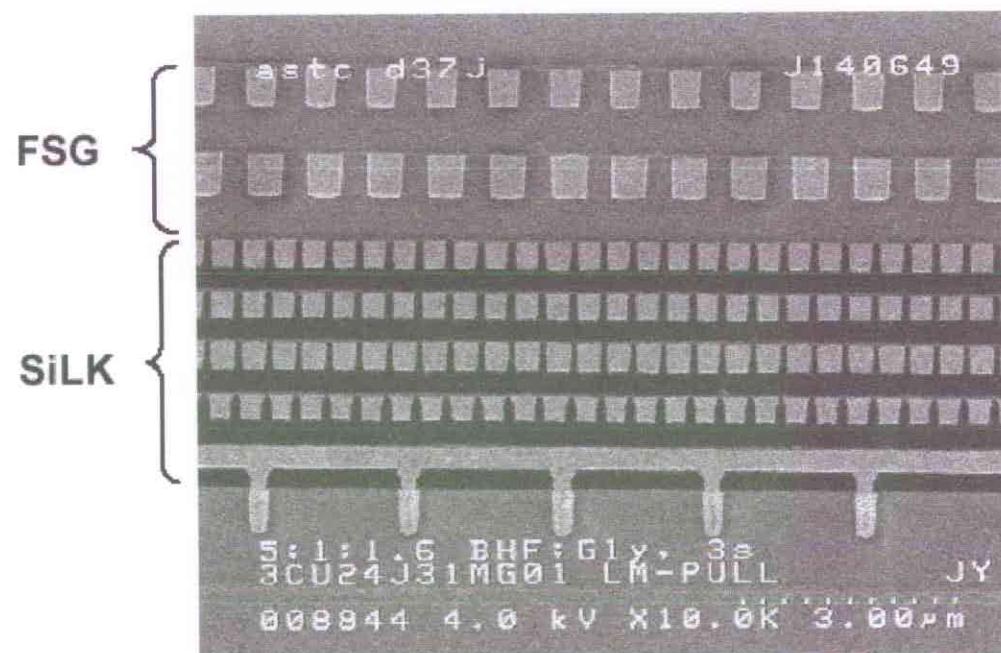
- 174 million transistors
- 8S2 (0.18 um) Technology

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## Up to 9 Layer Cu + SiLK Low-K

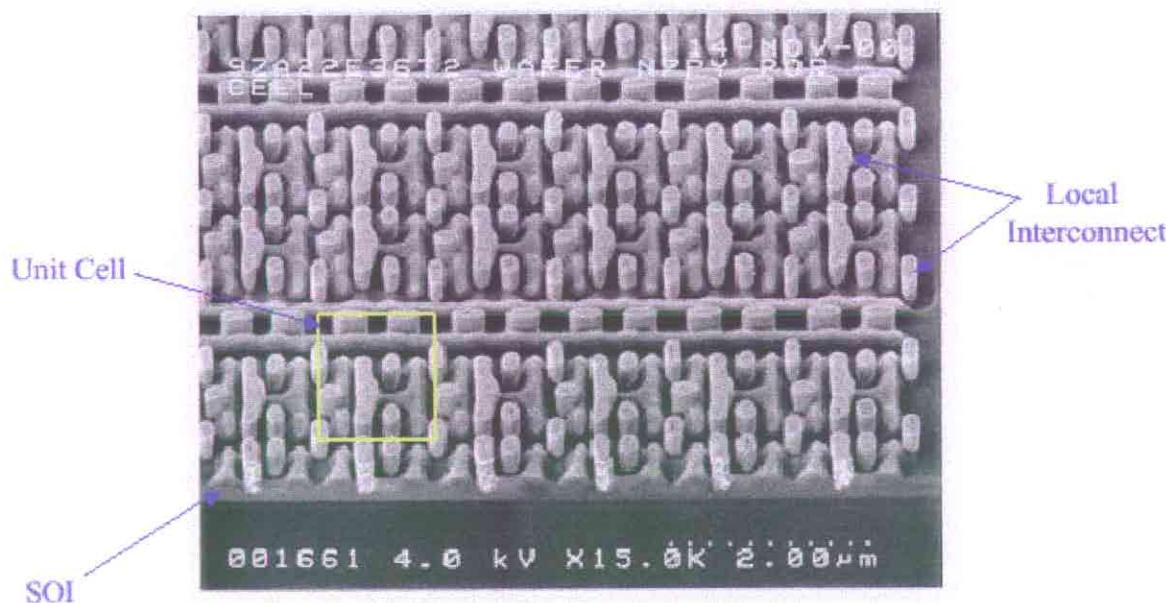


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## **2.16 $\mu\text{m}^2$ SRAM Cell**



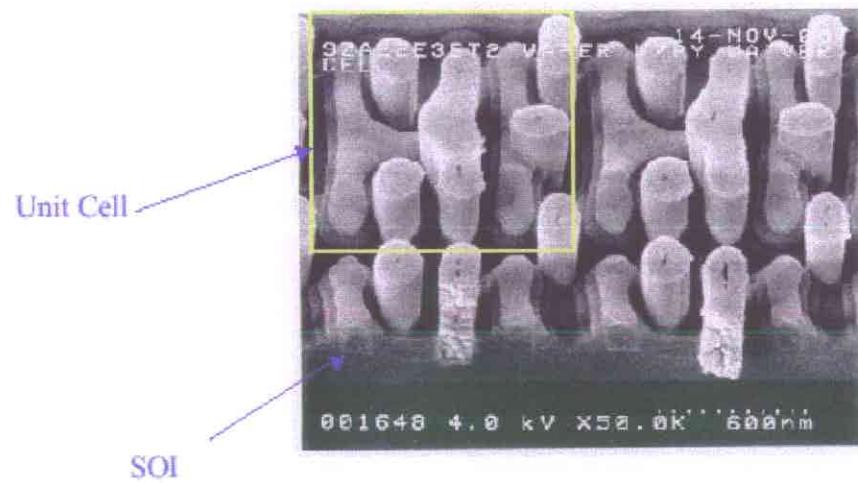
**In production in 2001**

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## **1.8 $\mu\text{m}^2$ SRAM Cell**



**In production in 2002**

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## 0.1 $\mu\text{m}$ CMOS Features

- *Silicon on Insulator*
  - 20-35% faster than bulk CMOS
  - 4<sup>th</sup> generation CMOS-SOI: Many SOI optimizations
- *Copper metalization*
  - 10 layers of metalization
  - 4<sup>th</sup> generation Copper in production
- *SiLK BEOL dielectric*
  - 2<sup>nd</sup> generation SiLK
  - Elimination of high K barrier levels (lower effective K)
- *Local interconnect (The only technology in the world)*
  - Smallest SRAM cell in the world

# **Advanced SOI Materials**

## **Patterned SOI**

## **Strained-Si/Si-Ge on SOI**

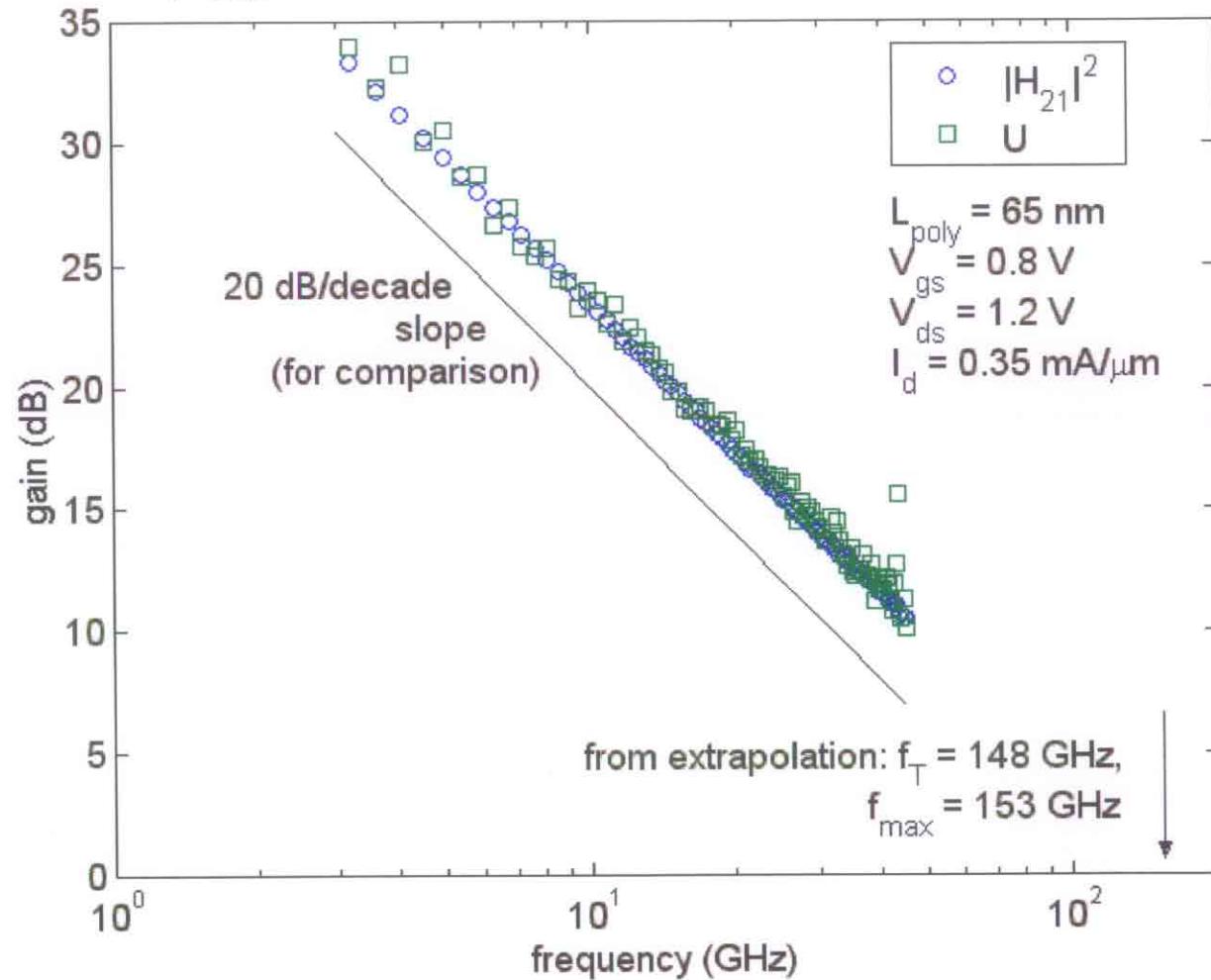
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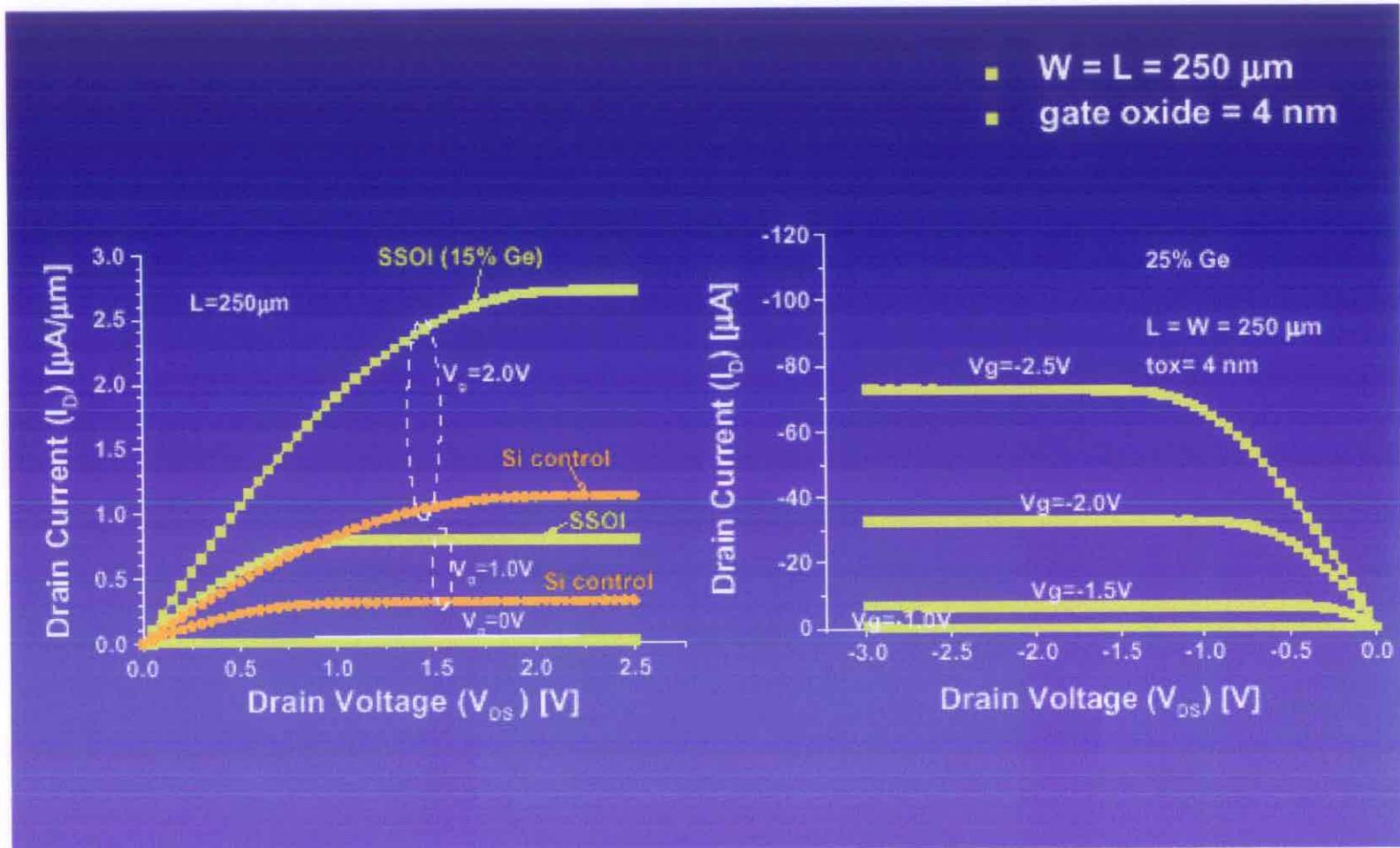
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# High $f_T$ nFET on SOI

Highest  $f_T$ ,  $f_{max}$  silicon FET ever measured: 9S lot 02C04SA, wafer MN1GKTY



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# **Future Directions**

## **SOI Thickness Roadmap**

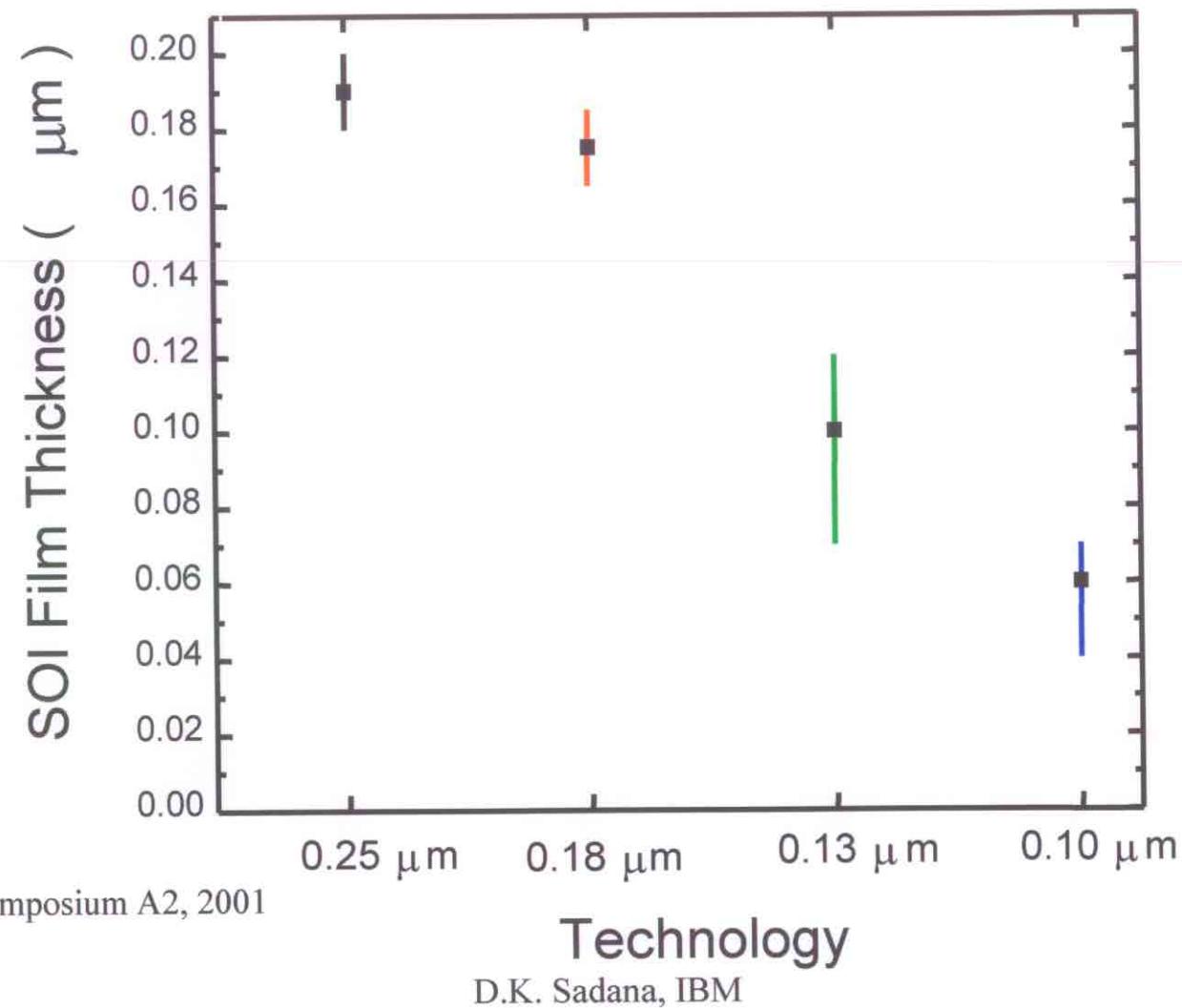
### **200/300mm Capacity**

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# SOI Film Thickness Roadmap



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